PENDING CLAIMS

1. (Previously presented) A DMA controller comprising:

at least one peripheral DMA channel for handling DMA transfers on a peripheral access bus;

at least one memory DMA stream, including a memory destination channel and a memory source channel, for handling DMA transfers on first and second memory access buses;

first and second address computation units for computing updated memory addresses for DMA transfers, wherein the first and second address computation units generate addresses at the same time to permit DMA transfer of data from one memory space to another memory space on the first and second memory access buses;

first and second memory pipelines for supplying memory addresses to the first and second memory access buses, respectively, and for transferring data on the first and second memory access buses; and

a multiplexer configured to supply first and second current memory addresses to selected ones of the first and second memory pipelines in response to a control signal.

2. (Original) A DMA controller as defined in claim 1, further comprising a peripheral prioritizer for prioritizing DMA requests for access to the peripheral access bus and a memory prioritizer for prioritizing DMA requests for access to one or both of the memory access buses.

3. (Original) A DMA controller as defined in claim 1, further comprising a traffic controller configured to give preference to consecutive transfers in one direction on one or more of the buses.

4. (Original) A DMA controller as defined in claim 1, wherein each of the peripheral DMA channels has a data FIFO with inputs receiving data from the peripheral access bus and the

memory access buses and with outputs supplying data to the peripheral access bus and the memory access buses.

5. (Original) A DMA controller as defined in claim 4, further comprising an urgent controller configured to increase the priority of a memory transfer when a peripheral DMA request is received and the data FIFO in a corresponding peripheral DMA channel is not ready to transfer data.

6. (Original) A DMA controller as defined in claim 4, wherein each of the one or more memory destination channels has a data FIFO with inputs receiving data from the memory access buses and with outputs supplying data to the memory access buses.

7. (Original) A DMA controller as defined in claim 1, wherein the multiplexer is configured to receive the first current memory address from one of the peripheral DMA channels or one of the memory destination channels and to receive the second current memory address from one of the memory source channels and to supply the first and second current memory addresses to selected ones of the memory pipelines.

8. (Original) A DMA controller as defined in claim 1, wherein each of the memory pipelines includes an address and write data pipeline for supplying memory addresses and write data to the respective buses, a read data pipeline for receiving read data from the respective buses and a control flow pipeline for controlling the flow of control information during a memory access.

9.-24. (Canceled)

25. (Previously presented) A DMA controller as defined in claim 1, wherein the DMA controller is programmable to transfer data from the peripheral access bus through the at least one

peripheral DMA channel and one of the memory pipelines to one of the memory access buses, to transfer data from one of the memory access buses through one of the memory pipelines and the at least one peripheral DMA channel to the peripheral access bus and to transfer data from one memory location to another memory location, through the memory source channel and the memory destination channel, between the first and the second memory access buses.

26. (Canceled)

27. (Previously presented) A DMA controller as defined in claim 1, wherein the multiplexer supplies the first and second current memory addresses to the first and second memory pipelines at the same time.